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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/965,458	09/27/2001	Franck Nozahic	PHFR 000103	5351

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EXAMINER	
RAMAKRISHNAIAH, MELUR	
ART UNIT	**PAPER NUMBER**
2643	

DATE MAILED: 12/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/965,458	NOZAHIC ET AL.	
	Examiner	Art Unit	
	Melur Ramakrishnaiah	2643	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 September 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5,9-11,14 and 15* is/are rejected.

7)☒ Claim(s) *6-8,12 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3-12-2002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claims 1-15 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claim 1-11 of U.S. Patent No. 6,703,901.

Although the conflicting claims are not identical, they are not patentably distinct from each other because for example claim 1 of the present application is an obvious variation of claim 1 of U.S. Patent No. 6,703,901.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5, 9-11, 14-15 are rejected under 35 U.S.C 102(b) as being anticipated by Lizong Sun et al. (Proceedings of the 1999 IEEE International Symposium On Circuits and Systems, Vol. 2, 30 May 1999, pages 152-155, XP-002168214, ISBN: 0-7803-5471-0, hereinafter Lizong Sun).

Regarding claim 1, Lizong Sun discloses a frequency synthesizer including a phase locked loop, which phase-locked loop comprises: a frequency divider (fig. 1) having integral dividing ratios, connected between a voltage controlled oscillator (VCO) and a phase frequency comparator (PFD, see fig. 1), a sigma-delta modulator (fig. 3) conned to frequency divider for commuting the dividing ratio of the frequency divider between a series of at least two integral values, so as to obtain a resulting mean dividing ratio with a fractional component, the modulator having at least one digital input suitable for receiving an adjusting instruction of the fractional component, means for fixing the value of at least significant bit of the adjusting instruction to 1 (page 152, column 1; page 153, column 1, line 23 –page 154, col. 2, line 15; figs. 1, 3, 5-7).

Regarding claim 9, Lizong Sun discloses a method of synthesizing frequency by means of a phase locking synthesizer comprising: a frequency divider (fig. 1) having integral dividing ratios, connected between a voltage controlled oscillator (fig. 1) and phase frequency comparator (PFD, fig. 1), a sigma-delta modulator (fig. 3) conned to frequency divider for commuting the dividing ratio of the frequency divider between a series of at least two integral values, so as to obtain a resulting mean dividing ratio that has a fractional component, the modulator having a digital input for an adjusting instructing the fractional component, and according to which an adjusting instruction is

formed for the sigma-delta modulator via a modification of a control input value, the input value being modified to make it odd value (page 152, column 1; page 153, column 1, line 23 –page 154, col. 2, line 15; figs. 1, 3, 5-7).

Regarding claims 2-5, 10-11, 14-15, Lizong Sun further teaches the following: having an input for a control value of the fractional component, and in which the means for fixing the value of the least significant bit to 1 comprises means for adding one bit equal to 1 to the control value of the fractional component and thus forming the adjusting instruction applied to the sigma-delta modulator, input register (figs. 5-6) of rank L-1 where L is an integer, and in which means for adding a bit equal to 1 comprises an instruction register of rank L, a locked flip-flop (fig. 5) for setting at least significant bit of the register of rank L to 1 and means for copying the control value in the instruction register of rank L as most significant bits, input register which has a control value of the fractional component, in which means for setting the value of the least significant bit of adjusting instruction to 1 comprises means for replacing the least significant bit of the control value by the value 1 and for applying this value to the modulator as an adjusting instruction, mixer (not shown) which has first input component connected to a signal source which delivers a signal with a frequency to be converted, and comprising a signal source which has a reference frequency connected to a second input of the mixer, characterized in that the signal source which has a reference frequency comprises a frequency synthesizer in a portable telephone (this arrangement is well known in the art in as much as the reference teaches using

frequency synthesizers in wireless transceivers; page 152, column 1; page 153, column 1, line 23 –page 154, col. 2, line 15; figs. 1, 3, 5-7).

5. Claims 6-8 and 12-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims (Note: this is subject to Applicant filing Terminal Disclaimer to overcome double patenting rejection set forth in item 2 above).

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

--(6,219,397) TO Park discloses a PLL-based CMOS fractional-N frequency synthesizer.

--(6,456,164) to Fan discloses Sigma Delta fractional-N frequency divider with improved noise and spur performance.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Melur Ramakrishnaiah whose telephone number is (571)272-8098. The examiner can normally be reached on 9 Hr schedule.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Curt Kuntz can be reached on (571) 272-7499. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Melur Ramakrishnaiah
Primary Examiner
Art Unit 2643